IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Jeff Brown

Serial No. : 10/028,582

Filed : December 20, 2001

For : Address Transition Detect Control Circuit For Self Timed Asynchronous Memories

Group Art Unit : 2818

Examiner : Pham, Ly D.

Atty Docket : 1496.00187 / 01-241

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

9/8/2005 Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 8 Sept 05

Respectfully submitted,

Timothy Croll

Reg. No. 36,771